

Low-Cost Coincidence Counting Apparatus For Single Photon Optics Investigations.

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Abstract: We have recently started investigating single photon experiments for our advanced laboratory and quantum mechanics classes. For a small department, the expenses of much of the apparatus is daunting. As such, we look for places where we can reduce the costs while still providing benefits for our students. One of the places where there can be some cost savings are in the coincidence counting unit. The coincidence counting unit is a critical piece of the investigation, and while not the most expensive component, cost savings are still available. We have developed a low-cost coincidence counter (less than \$50) based on a Cypress Programmable System on a Chip (PSoC). The PSoC is quite flexible and has both microcontroller as well as FPGA like capabilities which enable us to build the coincidence detection and the counter. The design process and several investigations will be presented.

Keywords: Quantum Optics, Single Photon, Coincidence Counter.

INTRODUCTION

Quantum Optics experiments have become very popular investigations in physics teaching laboratories. A rich body of investigations has been developed such as the Grainger experiment, Single Photon interference and the Quantum Eraser to name a few¹⁻⁵. These experiments allow students to learn about optics, interferometry, the fundamental nature of light, single photon detection, counting methods and quantum mechanics. In the course of working with single photon experiments, our students learn about different techniques for aligning optics and fiber optics as well as the fundamental optics. The increased interest in the single photon laboratories is, in part, due to the availability of lower cost Single Photon Avalanche Diode detectors (SPAD, ~\$5,000 for a set of four), lower cost coincidence detection, much more affordable laser systems (<\$100) and affordable down conversion crystals (BBO, ~\$500).

There have been a number of different coincidence counting units (CCU) developed of varying degrees of simplicity and cost. Notable are the several designs described in Branning et. al.^{6, 7} which have involved both discrete logic elements and an FPGA with a cost of \$300 or a more depending on how you do the configuration. References 8 and 9 presents designs solely based on an FPGA with time stamp features and a cost of approximately \$100. Reference 10 has several other designs.

For us, part of the process of learning about single photon experiments is to develop our own apparatus. The focus of the present work is to describe the

development of a lower cost and simpler coincidence detection system. Our design goals were to develop a relatively straightforward and simple system that required very little assembly but would be capable. What we came up with is a CCU with quad inputs and six counters, each capable of collecting up to four-fold coincidences based on a Cypress PSoC 5 microcontroller prototyping kit CY8CKIT-059 at a total cost of ~\$40.

WHAT IS A PSOC?

PSoC stands for Programmable System on a Chip. The PSoC 5 is a mixed signal microcontroller system. It comes with a 32 bit ARM Cortex M3 processor, a variety of analog components such as operational amplifiers, comparators, a 20 bit analog to digital converter, two 12 bit analog to digital converters, four digital to analog converters, a 24 bit digital filter system and 24 universal digital blocks (UDB). The UDB's consist of a matrix of uncommitted Programmable Logic Devices (PLD's) and a digital interconnect. The PLD may be configured to be any number of digital devices from simple logic elements to more complex digital devices such as counters, pulse width modulators and communication. Another interesting feature of the PSoC is that almost every pin is reconfigurable for analog or digital IO. Furthermore, Individual ports (a group of 8 pins) can be assigned different input/output voltages such as 1.2 V allowing convenient level shifting. One of the great advantages of the PSoC is that you can combine analog and digital circuitry on a single chip with a

relatively powerful processor which allows you to collect data and then do some processing on the data. Cypress has recently released the CY8CKIT-059 prototyping kit which makes using the PSoC 5 much simpler. Figure 1 shows an image of the CY8CKIT-059 prototyping kit. On the left side is the programmer which plugs directly into a USB port (or preferably a USB extension cable) and is also used for serial communications. Once your device is completely programmed, the programmer may be removed.



FIGURE 1. Photograph of the Cypress CY8CKIT-059 prototyping kit used in this project.

Programming the PSoC involves using free and downloadable, proprietary integrated development system from Cypress (for windows only, but works with a variety of virtual machines on different operating systems)- PSoC Creator^{11,12}. PSoC Creator allows you to graphically design the digital and analog components of the PSoC with drop and drag components (counters, PWM's, OpAmps, A/D converters, Capacitive sensors, etc.) and a wiring tool. Coding is completed in the environment using "c".

PSOC 5 COUNTER

The counter and coincidence detector that we developed has four, 50 ohm terminated input channels, six 24 bit counters, an adjustable window (0.1 s to 10s at present) and six outputs. The coincidence detection is programmable via capacitive buttons allowing any combination of inputs from single channels to four-fold coincidences to be counted. After each coincidence detection, the pulses are synchronized to the clock for counting. Each of the coincidence detectors also pass the pulses to each of six outputs which allow the counters to be combined to allow a greater number of inputs.

The coincidence detection is determined by the circuit shown in Figure 2. It consists of four OR gates to choose the inputs and an AND gate does the coincidence detection. The Control register is the interface between the processor and its firmware and the digital circuitry. If one of the control register bits is set high as one of the inputs for an OR gate, then the output of the OR gate will always be high and therefore that input will not matter.

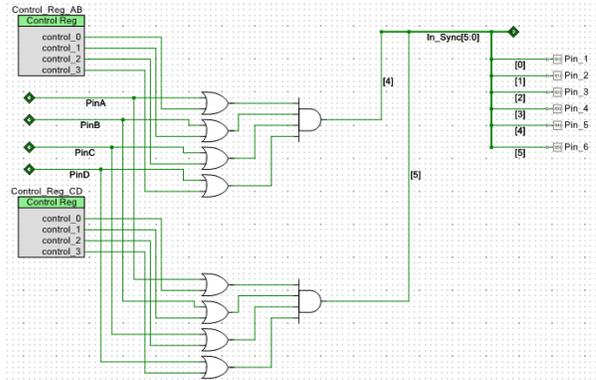


FIGURE 2. Section of the PSoC Counter showing the channel selection and coincidence detection circuitry. Control registers allow the CPU to interact with logic circuits through firmware. PinA – PinD are the inputs. Pin_1 – Pin_6 are the outputs. In_Sync[5:0] is a bus.

Similar to the design in Ref [9], we did not include pulse shaping into our system in part because our detectors generate 10 ns pulses and we felt that it was not necessary. However, this is something we can revisit at a later time.

We were able to use the counter by mounting the prototyping kit on an electronic breadboard. However, to make connections more secure we designed a simple two sided circuit board which was etched in the laboratory.

We found when using our SPAD's that the output is below TTL thresholds. We set the PSoC input to be LVTTTL, which is functional. However, as a future alternative, we will actually set the input voltage level on the prototyping kit using VDDIO.

The finished counter prototype is shown in Figure 3. All files, PSoC Creator files, EagleCad circuit board files, and interface software are available at Ref [13].

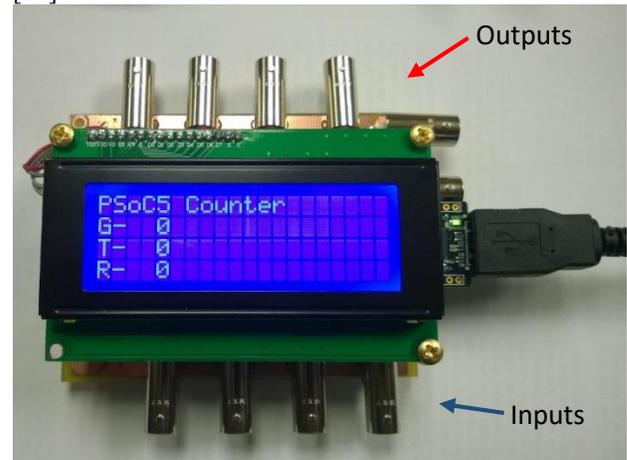


FIGURE 3. The completed counter system. The capacitive buttons are on the right hand side hidden by the LCD. The inputs are at the bottom. And the six outputs are on the top of the image. .

COUNTER AND COINCIDENCE TESTS.

To test the counter we initially used a pulse generator which allowed us to use pulses of 5 ns or longer. We used a 50MHz counter to compare the PSoC counter with measured counts. A 200 MHz oscilloscope was used to examine the pulses in and out of the PSoC counter. Our tests of the OR and AND gates indicate that they are very fast with very short propagation times (we measured differences in propagation times of less than 1 ns for 5 AND gates and 4 NOT gates). The largest propagation delays come from the input and output buffers. This is on the order of 35 ns. There was little distortion.

Figure 4 shows the counts for 10 ns pulses using the PSOC counter vs. the counts measured using the 50MHz counter as a function of input frequency. Exceeding 25 MHz, the PSoC counter is unable to keep up and starts to miss counts making it inaccurate and we do not consider it usable for more than 20MHz. We also found that for pulses shorter than 10 ns, the counter would miss counts. Therefore, the limitations we place on the device are a minimum pulse length of 10 ns and a maximum count rate of 2×10^7 cps. Since we are using 24 bit counters, the counting window so that we do not exceed 2^{24} counts or 1.678×10^7 counts. For low count rates we can use longer windows.

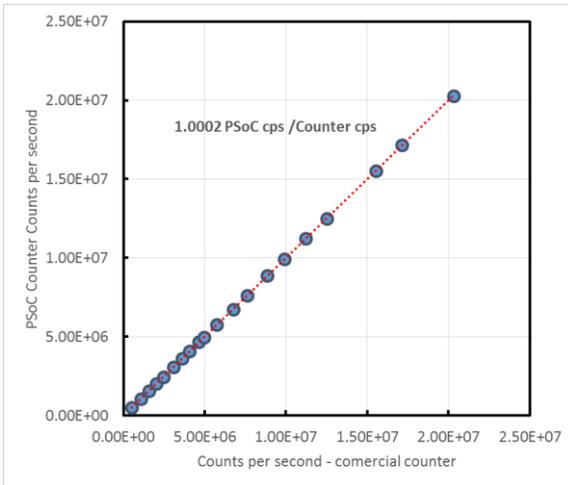


FIGURE 4. PSoC 5 Counter response vs. Commercial Counter. This indicates the counter is fairly well calibrated.

As a preliminary test of the counter, we assembled a dual channel pseudo random sequence (PRS) generator on a second PSoC 5 kit so that we could examine the response of the system using random inputs. As in Ref 2 and 6, the coincidences in two

random events has been shown to follow the form of $C = \tau \times R_1 R_2$, where C is the number of coincidences and R_1 is the counts on channel 1 and R_2 is the counts on channel 2. τ is the detection window. The data is shown in Figure 9 and yields a detection window of approximately 21.5 ns which is consistent with the pulse duration from our PRS.

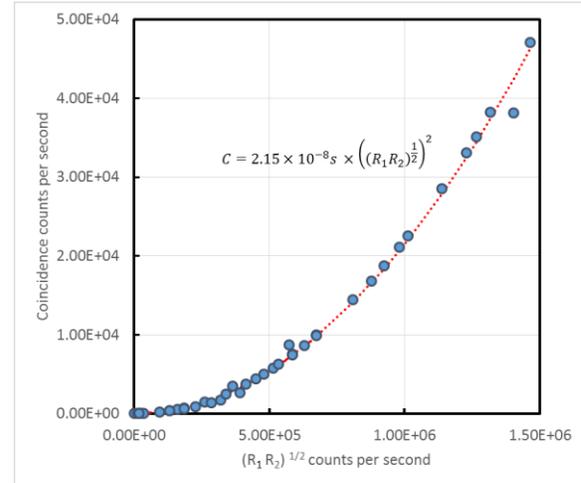


FIGURE 5. PSoC 5 Counter response to the two channel PRS. Analysis of this data indicates that the pulses generated by the PRS generator were approximately 21.5 ns since we do not make use of pulse shaping on the PSoC.

EXPERIMENTAL TESTS

As a final test of this counter, we put it into our single photon system. Since this is our first foray into quantum optics we are showing several simple tests as presented in Ref 2. Our experimental system is similar to the one described by Mark Beck¹⁴ with fiber coupled detectors and RG 780 filters in the path to protect the detectors.

In the first experiment, we use a small incandescent bulb (a random process) with ND filters and look at random coincidences between two detectors which allows us to determine the coincidence window. For the random thermal process we would expect the anticorrelation coefficient, $\alpha^{2d} = \frac{R_{AB}}{R_A R_B \tau}$ to be 1 (just as it was for the pseudo random pulse generator). In this expression, R_{AB} is the number of coincident counts per unit time, R_A and R_B are the counts per unit time of each of the detectors, and τ is the coincidence window. The 2d superscript indicates we are using two detectors as shown in Figure 6. Using this method, we find the coincidence window to be 10ns.

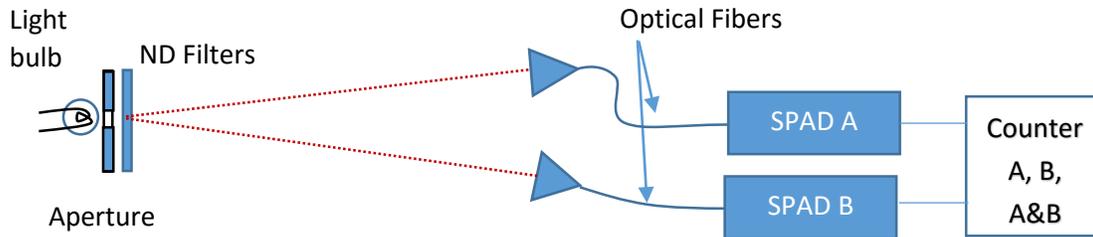


FIGURE 6. Setup with an incandescent light bulb to measure the coincidence window width which was 10.5 ns, in agreement with the pulse width from our SPAD's.

Finally, we performed a dual channel investigation using the nominally single photon source from a down conversion system. We hoped to measure an anti-correlation coefficient of much greater than 1. However, to date we have measured it to be 1.2, which is only two standard deviations above 1 and is rather disappointing. We currently attribute this failing to the pump laser which has a doughnut beam shape.

CONCLUSIONS

We have demonstrated a fairly simple counter which can be assembled for approximately \$40. Tests indicate that it is functional. While it presently is limited to four-fold detections, we have the ability to expand the number of inputs and outputs. What we cannot do is expand the number of counters without decreasing counter resolution to 16 bit. This could then greatly reduce the duration of the counting windows for high count rates. However, the system is scalable by combining several CCU's together.

There are improvements to be made to the system. A different circuit board design would place the capacitive buttons on the bottom of the circuit board and use the board as the lid to a box rather than an open frame system. It would also be helpful to utilize the onboard USB port rather than use the programmer for data communication. Data communication could be improved by better support software with graphical display – either through LabView or with a custom Python program. We also would like to add an SD card reader so that data can be stored directly on an SD card without the need for a computer.

At present we make little use of the processor on the microcontroller other than to read the counters, display the counts and then to send those to the computer. With a little effort we can have it collect statistics and report these as well.

Finally, we are considering developing our own circuit board, rather than depend on the prototyping kit because there are some advantages such as the ability to control the input levels of different ports. This would still be a one chip solution, however, the complexity of assembling such a system would be

quite a bit higher, requiring a more complex custom circuit board.

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